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| **Scenario**  You are a digital circuits designer, who is responsible for designing digital Training Kits for education. Your job duties include creating the logic system design, working with market customers to determine the type of digital modules needed in the kits, and troubleshooting errors in existing kit or products.  For a Digital Kit Product as shown in Figure (1). One kit model consists of a 4x4 Matrix Keypad, which receives code or sequence numbers (decimal numbers) from the trainee and converts outputs to binary output number. This output (binary) is then connected to a Digital Logic Processor (DLP), DLP is a specialized Microcontroller chip, with its architecture is optimized for carrying out logic functions. For a logic function takes three binary inputs named A, B, and C as input sequence with Least Significant Bit (LSB) for input A to the Most Significant Bit (MSB) for input C to that logic function. The output generates one-bit binary output Q. The output Q is stored in a memory one by one as a binary word or one byte (The Least Significant Bit (LSB) is at first). The binary output Q is processed by an arithmetic or logic process to displayed on LCD screen as a hexadecimal code as shown in the kit model.  The input sequence is **6325** decimal number.   * Each decimal number is processed to three logic inputs A, B, and C respectively. * The logic function is **Q = ( A’BC’ + A’B’C )’ .** |

**Model (**

**A**

**)**

**Model (B)**

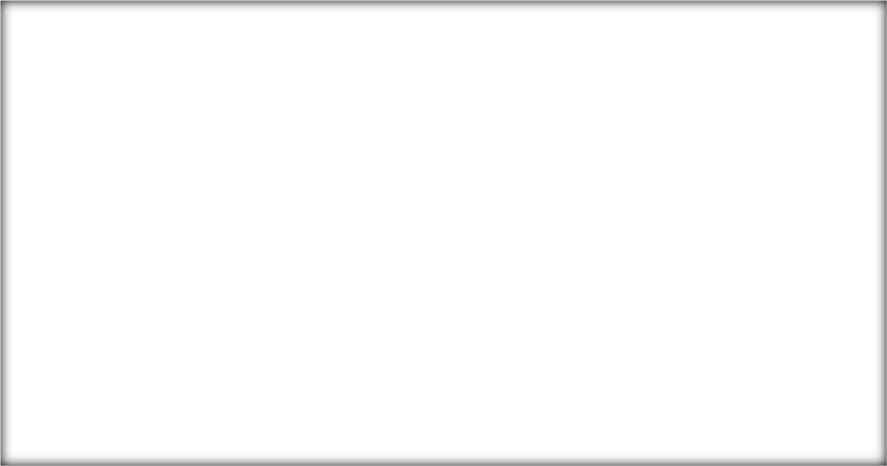
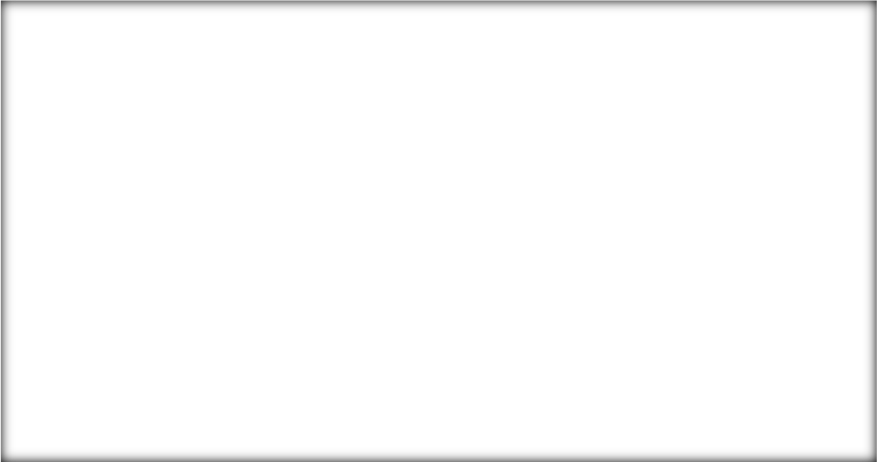
**Figure 1**

**D**

**igital**

**Kit**

**Product**



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| **Do the following Tasks:**    **Task 1:**   1. **Identify the main components of the given Digital Kit Products model (A) and Model (B) as shown in Figure (1), Compare and contrast between the two models, which one is described in the scenario.**   Kit (A) Components:   1. 4x4 Matrix Keyboard 2. Digital Logic Controller (DLC) 3. Arduino Uno, Consists of:  * Micro controller * Power input * Analog input * Power Supply  1. Cables and wires   Kit (B) Components:   1. Seven-Segment Mini Board 2. For the given logic function, explain its operation, make a good use of Boolean algebra and Truth Tables. And, sketch the logic diagram of the given logic function.   **Q = ( A’BC’ + A’B’C )’**  **Q = ( A+B’+C).(A+B+C’)**  Truth table:   |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | | A | B | C | A**’** | B**’** | C**’** | A+B**’**+C | A+B+C**’** | Q | | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |  |  |  |  |  |  |  |  |  |  1. **Convert the decimal input to the binary format. And the output to hexadecimal format.**   **Decimal to Binary:**  (6325)10 (1100010110101)2  6325 / 2 = 3162 R 1  3162 / 2 = 1581 R 0  1581 / 2 = 790 R 1  790 / 2 = 395 R 0  395 / 2 = 197 R 1  197 / 2 = 98 R 1  98 / 2 = 49 R 0  49 /2 = 24 R 1  24 / 2 = 12 R 0  12 / 2 = 6 R 0  6 / 2 = 3 R 0  3 / 2 = 1 R 1  1 / 2 = 0 R 1  **Binary to Hexadecimal:**  (1100010110101)2 (18B5)16  1 1000 1011 0101  1 8 4 2 1 8 4 2 1 8 4 2 1  1 8 11 5  1 8 B 5 |
| **4. Critically analyze the input and output methods for the Boolean expression of the given logic function when it has been processed using kit model (A) and model (B) in terms of component blocks in each kit as shown in Figure (1).** |

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| **Task 2:**  **1. Simplify the given logic function and write a step by step simplification process with Logic Rules. Then, check the simplified with the given function.**  Q = ( A’BC’ + A’B’C )’  (A’BC’) ’.(A’B’C) ’ (Apply DeMorgan’s Law)  (A’’+B’+C’’).(A’’+B’’+C’) (Involution Law x’’ = x)  (A+B’+C).(A+B+C’)   1. Identify the Minterm and Maxterm terms of the given logic function. 2. Represent the given logic function in terms of the Sum of Product (SOP) expression. 3. Use Karnaugh Map (K-Map) to simplify the given logic function. Then, check the simplified with the given function output. 4. Evaluate the simplification method according to the worst-case simplification scenario.     **Task 3: (In Lab Task)**   1. Use Multisim simulator to simulate the given logic function and to test its operation. 2. Use advanced input methods to simulate the given logic function and test its operation in each case using Multisim simulator. 3. Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario.      Printout the Logic diagram and its output.    **Sources of information**   * Class handouts and learning materials. * Individual research. * Lab …………. * <https://www.ekb.eg/> |

**Higher Nationals - Summative Assignment Feedback Form**

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| --- | --- | --- | --- | --- | --- | --- | --- |
| Student Name |  | | | | Student ID | |  |
| Unit Title |  | | | | | | |
| Assignment Number (1) |  | Assignment Title | |  | | | |
| Assessor Summative Feedback: Feedback should be against the learning outcomes and assessment criteria to help students understand how these inform the process of judging the overall grade. \*should be constructive and useful including:  - Feedback should give full guidance to the students on how they have met the learning outcomes and assessment criteria     1. Strengths of performance            1. Limitations of performance            1. Any improvements needed in future assessments | | | | | | | |
| Assessor Signature: | | | Date: / /2023 | | | | |
| Re-submission Date | / /2023 | | Actual Date Received Re- | | | | / /2023 |
| submission **Resubmission Feedback:**  \*Please note resubmission feedback is focussed only on the resubmitted work | | | | | | | |
| Assessor Signature: Date: / /2023 | | | | | | | |
| Internal Verifier’s Comments: | | | | | | | |
| Signature: | | | | | | Date: / /2023 | |

\* Please note that grade decisions are provisional. They are only confirmed once internal and external moderation has taken place and grades decisions have been agreed at the assessment board.

Summative Assignment Feedback Form

# Observation Sheet

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| Student Name and ID: | |  | | | |
| Unit Number and Title: | |  | | **Digital Engineering** | |
| Qualification | | Higher National Diploma in Information and Communications Technology (ICT) | | | |
| Assignment No. | **1** |  | Assignment Title: | | **Midterm - LO1 and LO2** |



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| **Description of the activity undertaken**   * **Use Multisim simulator to simulate the given logic function and to test its operation.** * **Use advanced input methods to simulate the given logic function and test its operation in each case using Multisim simulator.** * **Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario.**   **Observation Checklist**   |  |  |  |  | | --- | --- | --- | --- | | **The Observer will observe the student perform the following operation independently.**  Use Multisim simulator to do the following: | | | | | **Criteria Ref.** | **Task No.** | **Task Description** | **Tick if**  **met** | | **P6**  **M2**  **D1** | **3** | Navigate in Multisim Program and its Libraries for Logic gate simulation. |  | | Identify the suitable logic gates for the given logic function simulation. |  | | Select the appropriate inputs and outputs according to the logic function. |  | | Construct the complete logic and test the output for each input logic combination. |  | | Use advanced input methods to simulate the given logic function and test its operation in each case. |  | | Design a hardware implementation schematic and define the number of IC chips requirements for a Logic function implementation process in the given application scenario. |  | |

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| Observer Signature |  | Date |  |



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